**Low power VLSI Design Question Bank (EC0317)**

**Unit-1**

**1)** Explain the sources of power dissipation on Digital integrated circuits.

**2)** Discuss emerging low power approaches requires optimization at all design abstraction levels.

3) Explain the impact of technology scaling in CMOS.

4) What is the need for low power design in the VLSI circuits

5) Mention the source of power dissipation in the digital VLSI integrated circuits

6) How the Dynamic dissipation is dominant in CMOS circuits. What are the Techniques to reduce it.

7) How technology scaling is done in CMOS technology. What are its impact on device performance.

8) What are the innovative techniques developed in CMOS technology to improve its performance.

9) Explain transistor sizing and gate oxide thickness impact on device performance.

10) Explain technology and device innovation techniques developed in CMOS.

**Unit-2**

1. Discuss the effect of different switching probabilities at different nodes in a circuit.
2. Explain the effects of circuit capacitance for power consumption.
3. Discuss the power consumption in static and dynamic flip-flops taking an example of D-flip-flop.
4. Discuss the power consumption in static and dynamic flip-flops taking an example of D-flip-flop using Transmission gates.
5. Explain the possibilities to reduce power consumption for large capacitive loads.
6. Discuss low power digital cell library with respect to cell sizes and spacing.
7. Explain gate reorganization with necessary logic diagram
8. Discuss signal gating with relevant diagrams.
9. Explain logic encoding with relevant logic table.
10. Discuss state machine encoding techniques to reduce low power consumption.

**Unit-3**

1. Explain the characterization of continuous and discrete random logic

Signals.

1. Explain the expected frequency and static probabilities of discrete random logic signals.
2. Discuss the characterization of logic signals
3. Discuss the conditional probability and frequency with necessary equations.
4. Explain the probabilistic power analysis techniques with logic diagram
5. Discuss the propagation of stastical quantitates in probabilistic power analysis techniques
6. Compute the transition density and static probability of y=ab+c given P(a)=0.2, P(b)=0.3,P(c)=0.4,D(a)=1, D(b)=2,D(c)=3.

**Unit-4**

1. Discuss how the pipelining and parallelism techniques are used to reduce power dissipation at architecture level.
2. Explain with block diagram the adaptive performance management by voltage control.
3. Discuss switching activity reduction with block diagram
4. guarded evaluation
5. bus multiplexing
6. Explain flow graph transformation with neat block diagram
7. operator reduction
8. loop Unrolling
9. Explain with design flow and some supporting tools for proposed low power CAD frame work.

**Unit-5**

1. Mention the advantage and limitations of the spice power analysis method
2. Explain the effects of data correlation on bit switching frequency.
3. Mention the steps to obtain total power dissipation of the circuit after conducting the gate level power simulation
4. Explain the spice power analysis
5. Discuss the gate level logic simulation with equations.
6. Explain the architecture level analysis with respect to
7. Power models based on activities
8. Power models based on component operations

7. Discuss the Data correlation analysis in DSP systems.

**Unit-6**

1. Distinguish between conventional charging and adiabatic charging of load capacitance
2. Explain how dynamic power dissipation is minimized using adiabatic switching.
3. Explain basic steps of battery aware task scheduling. How does it improves the life time of a battery
4. Discuss adiabatic charging principle with equations
5. Explain adiabatic amplifier circuit with equations.
6. Explain variation tolerant design techniques

**SLE**

1. Draw the energy band diagram of MIS (metal insulator semiconductor) structure for accumulation region operation of PMOS device.
2. Draw the energy band diagram of MIS (metal insulator semiconductor) structure when negative bias applied
3. Draw the energy band diagram of MIS (metal insulator semiconductor) structure when positive bias applied
4. Mention how precomputation logic helps to reduce power dissipation at gate level design with an example.
5. The standard deviation of the power samples measured from a circuit has been observed to have +/-20% fluctuation from the mean. Compute how many samples are required so that we are 99% confidence that the error of sample mean is within +/-5%.
6. What is the limitation of contemporary CAD tools.
7. Discuss the importance of Monte Carlo simulation
8. Discuss the application of signal entropy
9. Discuss precomputation logic with necessary schematic diagrams